AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-2 (canceled)

Claim 3 (currently amended) A semiconductor integrated circuit device, comprising:

a source region formed on a semiconductor substrate;

a first conductor having a first resistivity formed over said source region;

a first contact group having a plurality of first contacts connecting said source region and said first conductor, the first contacts being formed over said source region;

a second conductor having a second resistivity over said first conductor;

a second contact group having a plurality of second contacts connecting said first conductor and said second conductor, the second contacts being formed over said source region;

a drain region formed on said semiconductor substrate;

a third conductor having said first resistivity formed over said drain region;

a third contact group having a plurality of third contacts connecting said drain region and said third conductor, the third contacts being formed over said drain region;

a fourth conductor having said second resistivity formed over said third conductor;

a fourth contact group having a plurality of fourth contacts connecting said third conductor and said fourth conductor, the fourth contacts being formed over said drain region;

wherein a total number of the first contacts ~~in said first contact group~~ is different from a total number of the second contacts ~~in said second contact group~~, and a total number of the third contacts ~~in~~

~~said third contact group~~ is different from a total number of the fourth contacts ~~in said fourth contact group~~.

Claim 4 (previously presented) The semiconductor integrated circuit device as claimed in claim 3, wherein the total number of contacts in said first contact group is the same as the total number of contacts in said third contact group, and the total number of contacts in said second contact group is the same as the total number of contacts in said fourth contact group.

Claim 5 (previously presented) The semiconductor integrated circuit device as claimed in claim 4, wherein said first resistivity is higher than said second resistivity, and a total number of contacts in said first contact group and in said third contact group is greater than a total number of contacts in said second contact group and in said fourth contact group.

Claim 6 (currently amended) A semiconductor integrated circuit device, comprising:

a first impurity diffusion region and a second impurity diffusion region formed on a semiconductor substrate, extending in a first direction and standing side by side in a second direction;

a first conductor having a first resistivity formed over said first impurity diffusion region;

a first contact group, having a plurality of first contacts arranged side by side in said first direction over said first impurity diffusion region, for connecting said first impurity diffusion region and said first conductor;

a second conductor having a second resistivity formed over said first conductor;

a second contact group, having a plurality of second contacts arranged side by side in said first direction over said first impurity diffusion region, for connecting said first conductor and said second conductor;

a third conductor having said first resistivity formed over said second impurity diffusion region;

a third contact group, having a plurality of third contacts arranged side by side in said first direction over said second impurity diffusion region, for connecting said second impurity diffusion region and said third conductor;

a fourth conductor having said second resistivity formed over said third conductor; and

a fourth contact group, having a plurality of fourth contacts arranged side by side in said first direction over said second impurity diffusion region, for connecting said third conductor and said fourth conductor, wherein said first contact group is arranged between neighboring contacts of said second contact group, and

wherein said third contact group is arranged between neighboring contacts of said fourth contact group.

Claim 7 (previously presented) The semiconductor integrated circuit device as claimed in claim 6, wherein

a distance between a contact of said first contact group and a contact of said second contact group adjacent to the contact of said first contact group is a fixed value, and

a distance between a contact of said third contact group and a contact of said fourth contact group adjacent to the contact of said third contact group is a fixed value.

Claim 8 (previously presented) The semiconductor integrated circuit device as claimed in claim 6, wherein

an interval between contacts of said first contact group situated between neighboring contacts of said second contact group is a fixed value, and

an interval between contacts of said third contact group situated between neighboring contacts of said fourth contact group is a fixed value.

Claim 9 (previously presented) The semiconductor integrated circuit device as claimed in claim 6, wherein

said first impurity diffusion region has

a first side and a second side running in said second direction,

a third side running in said first direction and opposite to said second impurity diffusion region,

a first distance defined as a distance from said first side to an edge of said first contact group extremely close to said first side,

a second distance defined as a distance from said second side to an edge of said first contact group extremely close to said second side, and

a third distance defined as a distance from said third side to an edge of said first contact hole group extremely close to said third side,

said second impurity diffusion region has

a fourth side and a fifth side running in said second direction,

a sixth side running in said first direction and opposite to said first impurity diffusion region,

a fourth distance defined as a distance from said fourth side to an edge of said third contact group extremely close to said fourth side,

a fifth distance defined as a distance from said fifth side to an edge of said third contact group extremely close to said fifth side, and

a sixth distance defined as a distance from said sixth side to an edge of said third contact group extremely close to said sixth side,

said first distance and said second distance are both larger than said third distance, and

said fourth distance and said fifth distance are both larger than said sixth distance.

Claim 10 (previously presented) The semiconductor integrated circuit device as claimed in claim 6, wherein

said first contact group is divided into a plurality of subgroups each having a predetermined fixed number of contacts, and each subgroup is arranged between adjacent contacts of said second contact group, and

said third contact group is divided into a plurality of subgroups each having a predetermined fixed number of contacts, and each subgroup is arranged between adjacent contacts of said fourth contact group.

Claim 11 (previously presented) The semiconductor integrated circuit device as claimed in claim 10, wherein

a distance from contacts of said first contact group and contacts of said second contact group adjacent to contacts of said first contact group, has a fixed value, and

a distance from contacts of said third contact group and contacts of said fourth contact group adjacent to contacts of said third contact group, has a fixed value.

Claim 12 (previously presented) The semiconductor integrated circuit device as claimed in claim 10, wherein

an interval between contacts of said first contact group arranged between adjacent contacts of said second contact group has a fixed value, and

an interval between contacts of said third contact group arranged between adjacent contacts of said fourth contact group has a fixed value.

Claim 13 (previously presented) The semiconductor integrated circuit device as claimed in claim 10, wherein

said first impurity diffusion region has

a first side and a second side running in said second direction,

a third side running in said first direction and opposite to said second impurity diffusion region,

a first distance defined as a distance from said first side to an edge of said first contact group extremely close to said first side,

a second distance defined as a distance from said second side to an edge of said first contact group extremely close to said second side, and

a third distance defined as a distance from said third side to an edge of said first contact hole group extremely close to said third side,

said second impurity diffusion region has

a fourth side and a fifth side running in said second direction,

a sixth side running in said first direction and opposite to said first impurity diffusion region,

a fourth distance defined as distance from said fourth side to an edge of said third contact group extremely close to said fourth side,

a fifth distance defined as a distance from said fifth side to an edge of said third contact group extremely close to said fifth side, and

a sixth distance defined as a distance from said sixth side to an edge of said third contact group extremely close to said sixth side,

said first distance and said second distance are both larger than said third distance, and

said fourth distance and said fifth distance are both larger than said sixth distance.

Claim 14 (currently amended) A semiconductor integrated circuit, comprising a first transistor for input and a second transistor for output, said first transistor and said second transistor being connected to an input/output terminal, wherein

said first transistor includes

a first impurity diffusion region and a second impurity diffusion region formed on a semiconductor substrate, extending in a first direction and standing side by side in a second direction;

a first conductor having a first resistivity formed over said first impurity diffusion region;

a first contact group, having a plurality of first contacts arranged side by side in said first direction over said first impurity diffusion region, for connecting said first impurity diffusion region and said first conductor;

a second conductor having a second resistivity formed over said first conductor;

a second contact group, having a plurality of second contacts arranged side by side in said first direction over said first impurity diffusion region, for connecting said first conductor and said second conductor;

a third conductor having said first resistivity formed over said second impurity diffusion region;

a third contact group, having a plurality of third contacts arranged side by side in said first direction over said second impurity diffusion region, for connecting said second impurity diffusion region and said third conductor;

a fourth conductor having said second resistivity formed over said third conductor; and

a fourth contact group, having a plurality of fourth contacts arranged side by side in said first direction over said second impurity diffusion region, for connecting said third conductor and said fourth conductor,

wherein said first contact group has a predetermined fixed number of the first contacts arranged between each of the neighboring ~~contact of said~~ second contacts ~~contact group~~, and has a first fixed interval between said ~~predetermined number of arranged~~ first contacts ~~and adjacent contacts~~ and said third contact group has a predetermined fixed number of the third contacts arranged between each of the neighboring ~~contact of said~~ fourth contacts ~~contact group~~, and has said first fixed interval between said ~~predetermined number of arranged~~ third contacts ~~and adjacent contacts~~, and

wherein said second transistor includes

a third impurity diffusion region and a fourth impurity diffusion region formed on said semiconductor substrate, extending in a third direction and standing side by side in a fourth direction;

a fifth conductor having said first resistivity formed over said third impurity diffusion region;

a fifth contact group, having a plurality of fifth contacts arranged side by side in said third direction over said third impurity diffusion region, for connecting said third impurity diffusion region and said fifth conductor;

a sixth conductor having said second resistivity formed over said fifth conductor;

a sixth contact group, having a plurality of sixth contacts arranged side by side in said third direction over said third impurity diffusion region, for connecting said fifth conductor and said sixth conductor;

a seventh conductor having said first resistivity formed over said fourth impurity diffusion region;

a seventh contact group, having a plurality of seventh contacts arranged side by side in said third direction over said fourth impurity diffusion region, for connecting said fourth impurity diffusion region and said seventh conductor;

an eighth conductor having said second resistivity formed over said seventh conductor; and

an eighth contact group, having a plurality of eighth contacts arranged side by side in said third direction over said fourth impurity diffusion region, for connecting said seventh conductor and said eighth conductor,

wherein said fifth contact group has a predetermined fixed number of fifth contacts arranged between each neighboring sixth contact ~~of said sixth contact group~~, and has said first fixed interval between said ~~predetermined number of arranged~~ fifth contacts ~~and adjacent contacts~~, and said seventh contact group has a predetermined fixed number of seventh contacts arranged between each of the neighboring ~~contact of said~~ eighth contacts ~~contact group~~, and has said first fixed interval between said ~~predetermined number of arranged~~ seventh contacts ~~and adjacent contacts~~.

Claim 15 (previously presented) The semiconductor integrated circuit as claimed in claim 14, having

a first side, for said first impurity diffusion region, running in said first direction and opposite to said second impurity diffusion region;

a second side, for said second impurity diffusion region, running in said first direction and opposite to said first impurity diffusion region;

a third side, for said third impurity diffusion region, running in said third direction and opposite to said fourth impurity diffusion region;

a fourth side, for said fourth impurity diffusion region, running in said third direction and opposite to said third impurity diffusion region;

a first distance defined as a distance between said first side and said second side; and

a second distance defined as a distance between said third side and said fourth side,

wherein said first distance and said second distance are equal.

Claim 16 (currently amended) A transistor for use in an input protection circuit that protects circuitry fabricated on a semiconductor substrate, said transistor comprising:

a source region formed on the semiconductor substrate;

a first conductor having a first resistance formed over the source region;

a first number of first contacts connecting said source region and said first conductor;

a second conductor having a second resistance which is lower than the first resistance, said second conductor being formed over said first conductor;

a second number of second contacts connecting said first and second conductors, formed over said source region;

a drain region formed on the semiconductor substrate;

a third conductor having the first resistance formed over the drain region;

a third number of third contacts connecting said drain region and said third conductor;

a fourth conductor having the second resistance formed over said third conductor;

a fourth number of fourth contacts connecting said third and fourth conductors, formed over said drain region;

a gate insulating layer formed on the semiconductor substrate between said source and drain regions; and

a gate electrode formed on the gate insulating layer,

wherein the first number is more than twice as large as the second number, and

wherein the third number is more than twice as large as the fourth number.

Claim 17 (previously presented) A transistor according to claim 16, wherein the first number is equal to the third number and the second number is equal to the fourth number.

Claim 18 (previously presented) A transistor according to claim 16, wherein said second contacts are located over end portions of said source region and said first contacts holes are located over a central portion of said source region.

Clam 19 (previously presented) A transistor according to claim 16, wherein said fourth contacts are located over end portions of said drain region and said third contacts are located over a central portion of said drain region.

Claim 20 (previously presented) A transistor according to claim 16, wherein a distance from an end of the source region to a nearest one of the first contacts is equal to or greater than a distance from the gate electrode to said nearest one of the first contacts.

Claim 21 (previously presented) A transistor according to claim 16, wherein a distance from an end of the drain region to a nearest one of the third contacts is equal to or greater than a distance from the gate electrode to said nearest one of the third contacts.